Πανεπιστήμιο Πατρών

Τμήμα Φυσικής

Εργαστήριο Ηλεκτρονικής

Phase-Locked Loops (PLLs)

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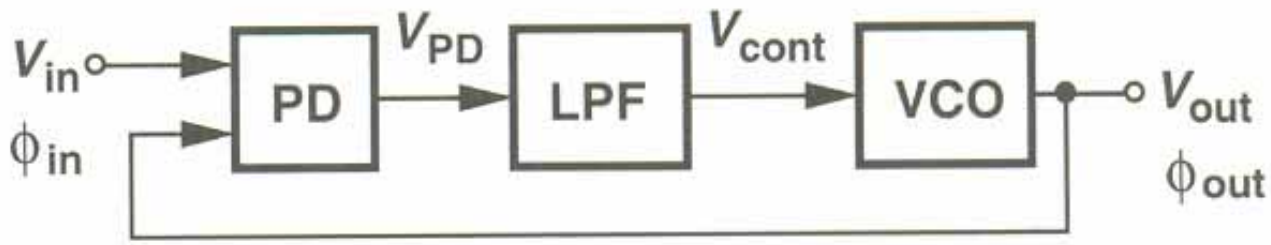
1.Εισαγωγή

Το PLL είναι ένας βρόχος ανατροφοδότησης όπου γίνεται σύγκριση της φάσης στην έξοδο, με τη φάση στην είσοδο.

Αυτή γίνεται από έναν συγκριτή φάσης (phase comparator or phase detector-PD).



(b)

Phase Detector

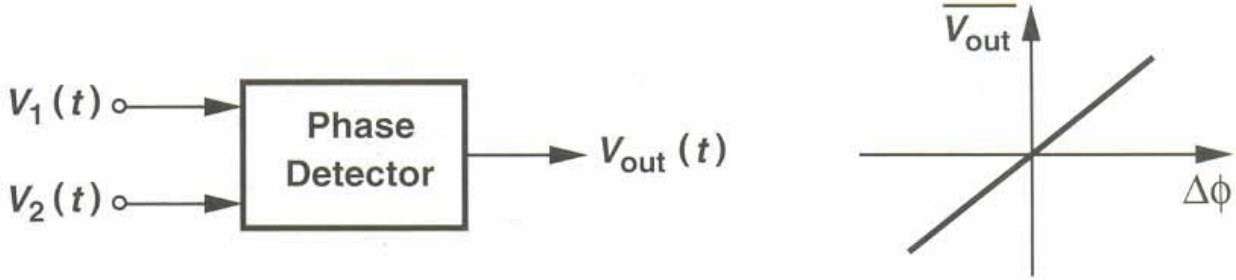


Figure 15.1 Definition of phase detector.

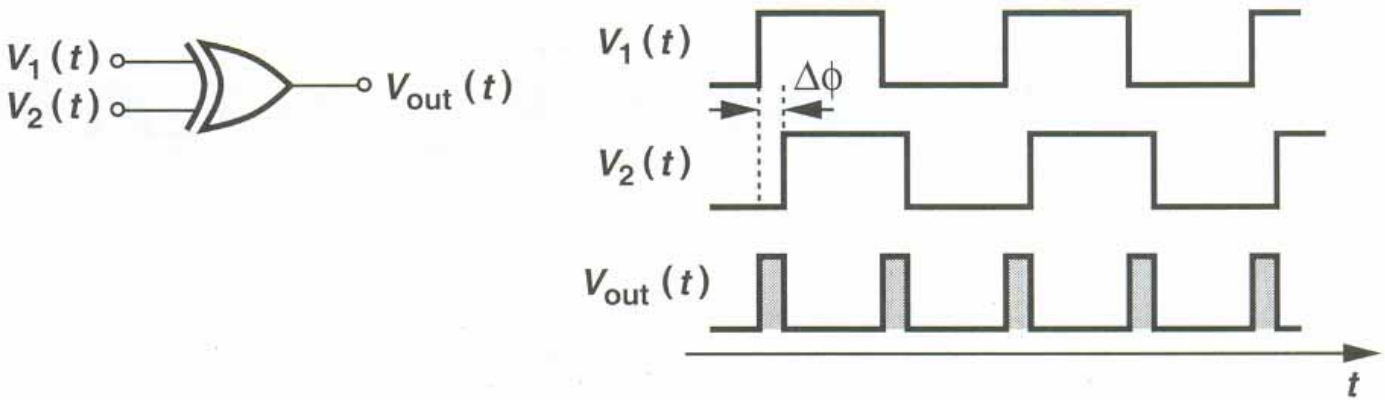
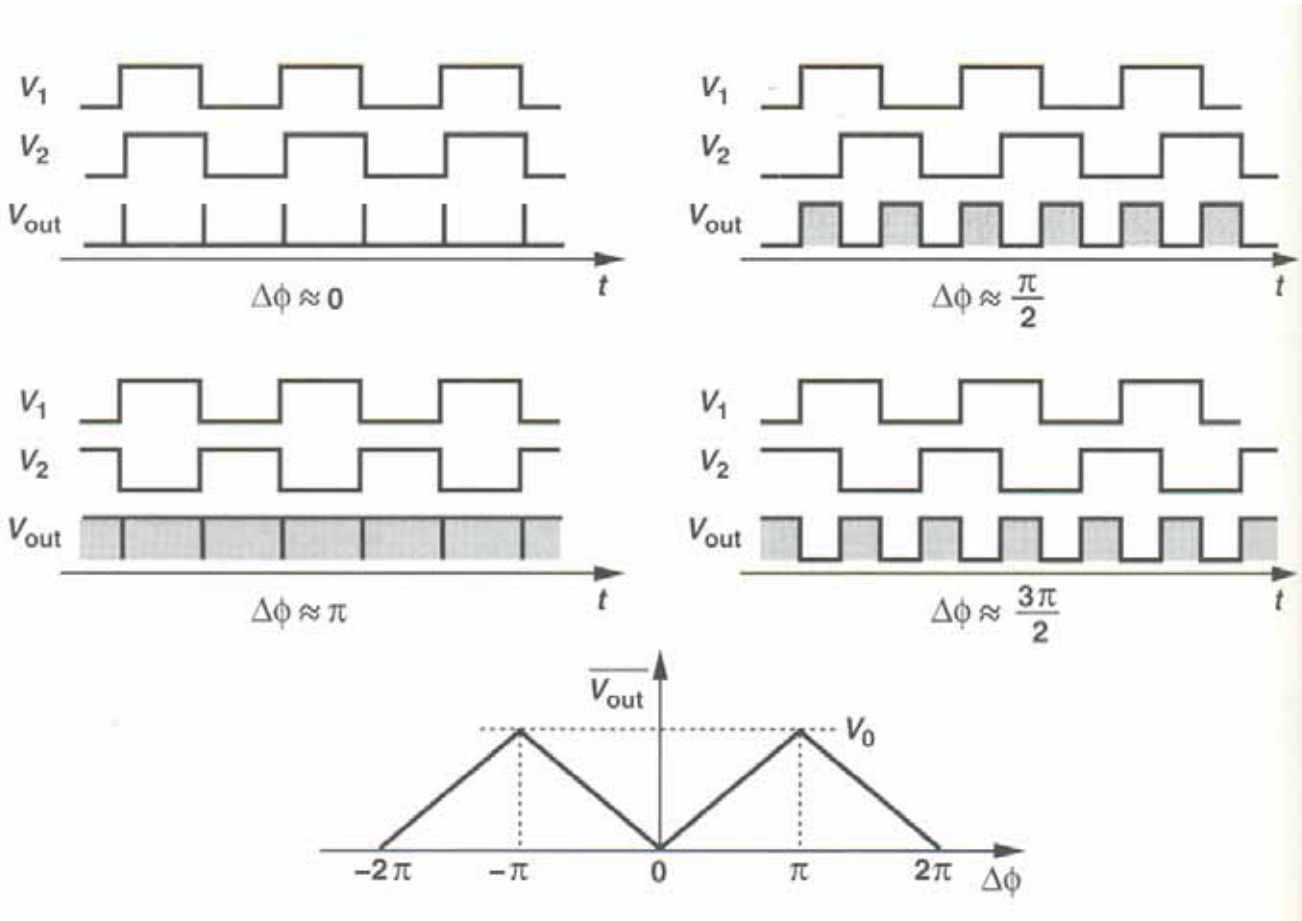
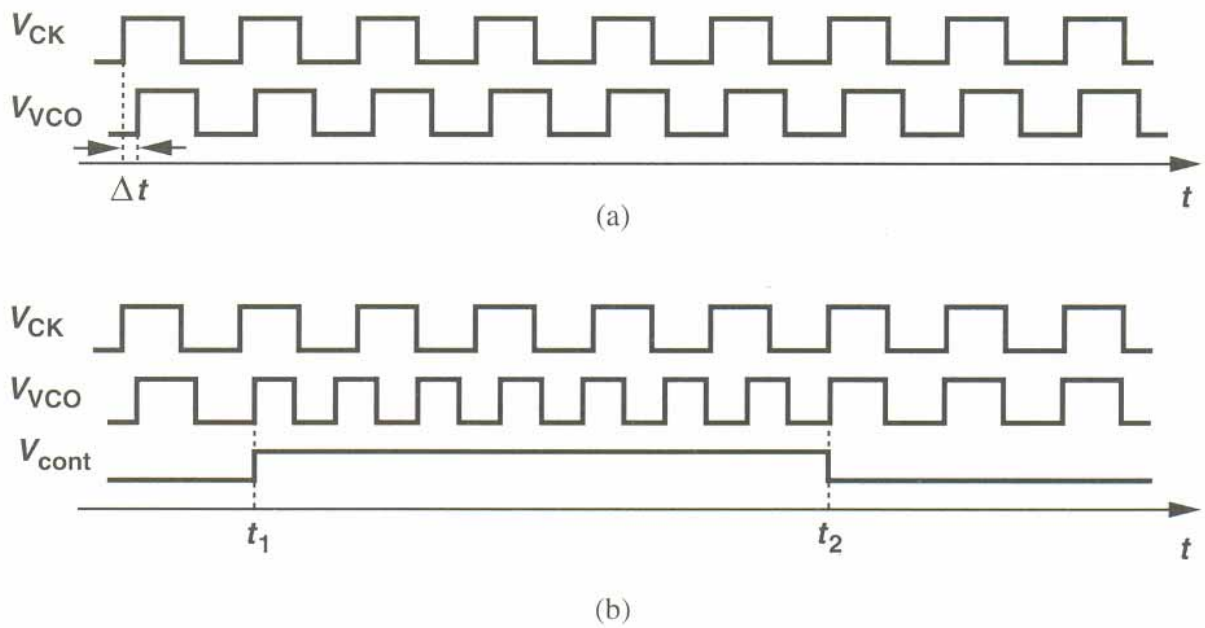


Figure 15.2 Exclusive OR gate as phase detector.

Input-Output characteristic of a PLL



Συγχρονισμός της φάσης δύο σημάτων



Η φάση εξόδου ενός PLL μπορεί να συγχρονιστεί (aligned) με τη φάση του σήματος αναφοράς εάν:

•Χρησιμοποιηθεί ένας ανιχνευτής φάσης για να καθορίζει πότε τα δύο σήματα είναι συγχρονισμένα.

•Αλλάξει στιγμιαία η συχνότητα του VCO.

Phase lock condition

$$\phi_{out} - \phi_{in} = const.$$

$$\frac{d\phi_{out}}{dt} - \frac{d\phi_{in}}{dt} = 0$$

$$\omega_{out} = \omega_{in}.$$

✓<u>In summary, when locked, a PLL produces an output that has a small phase error with respect to the input but exactly the same frequency</u>

PLL Waveforms in Locked Condition

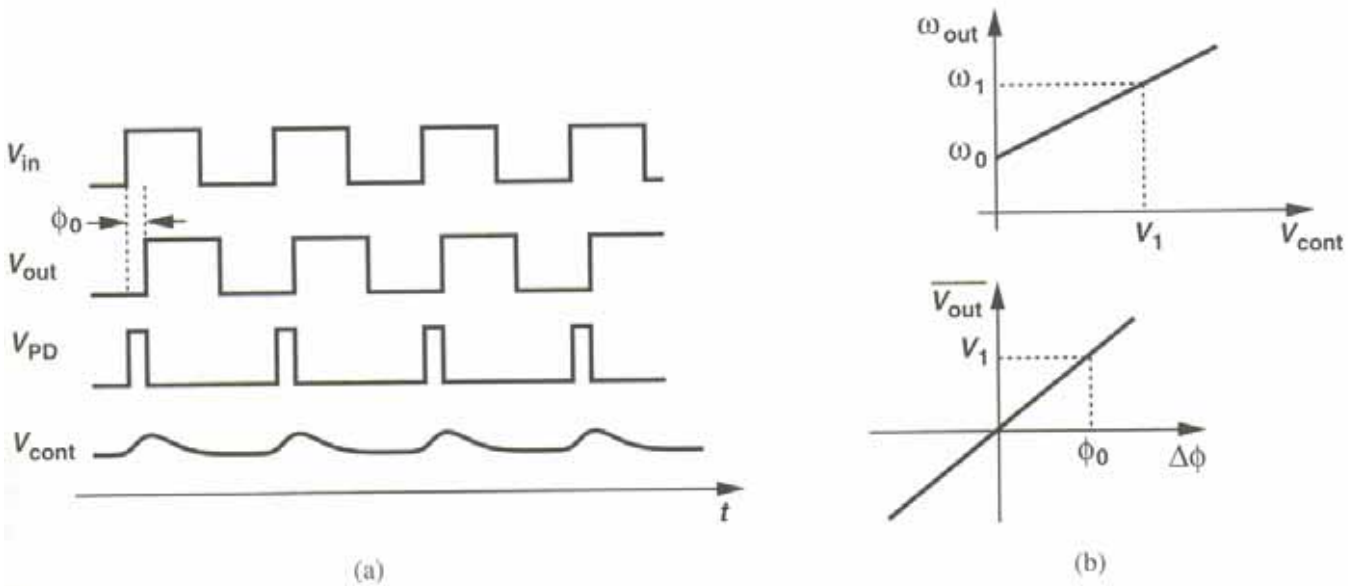


Figure 15.7 (a) Waveforms in a PLL in locked condition, (b) calculation of phase error.

$$V_1 = \frac{\omega_1 - \omega_0}{K_{VCO}}, \tag{15.3}$$

and

$$\phi_0 = \frac{V_1}{K_{PD}} \tag{15.4}$$

$$= \frac{\omega_1 - \omega_0}{K_{PD} K_{VCO}}. \tag{15.5}$$

Equation (15.5) reveals two important points: (1) as the input frequency of the PLL varies, so does the phase error; (2) to minimize the phase error, $K_{PD} K_{VCO}$ must be maximized.

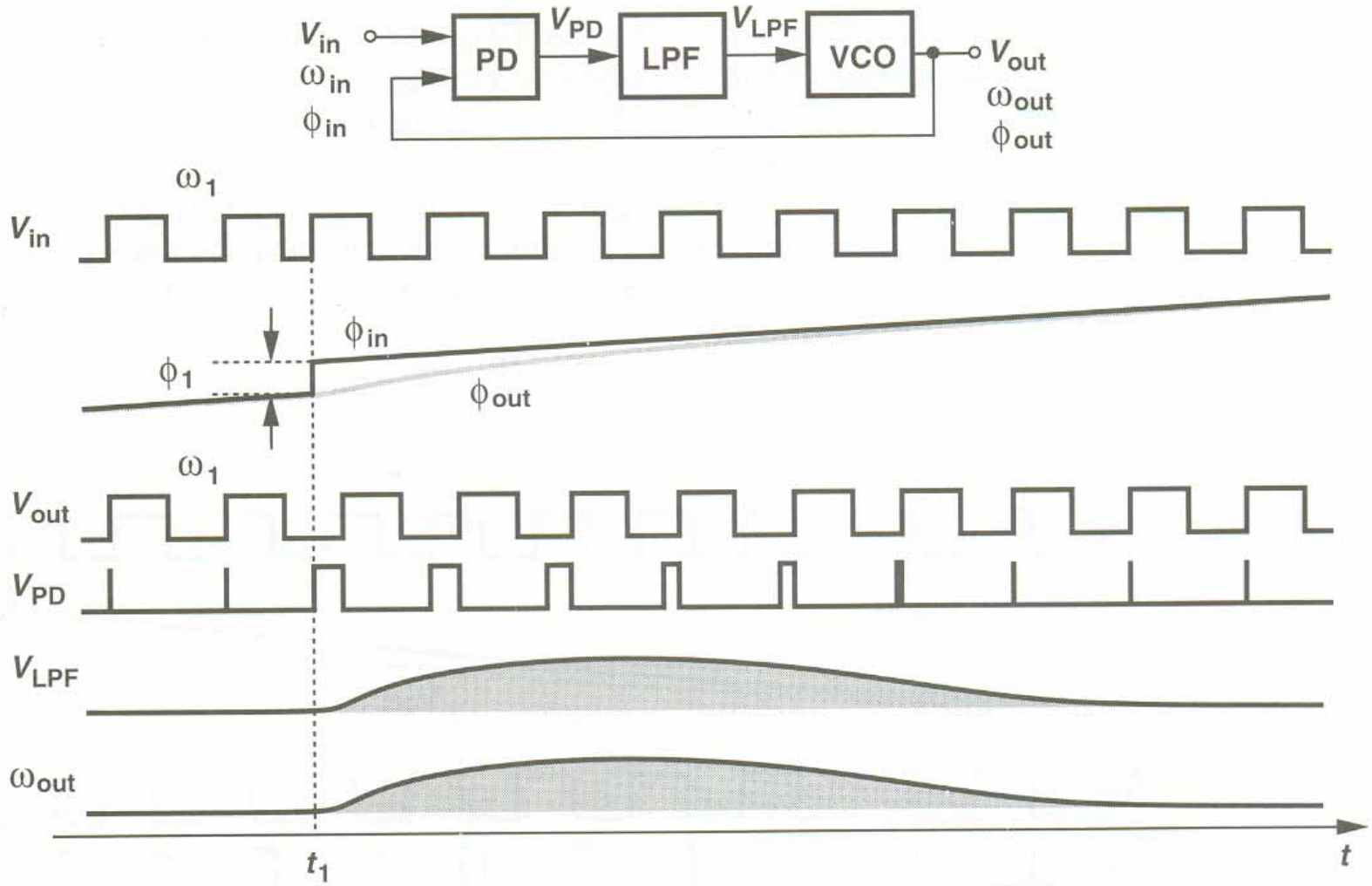


Figure 15.11 Response of a PLL to a phase step.

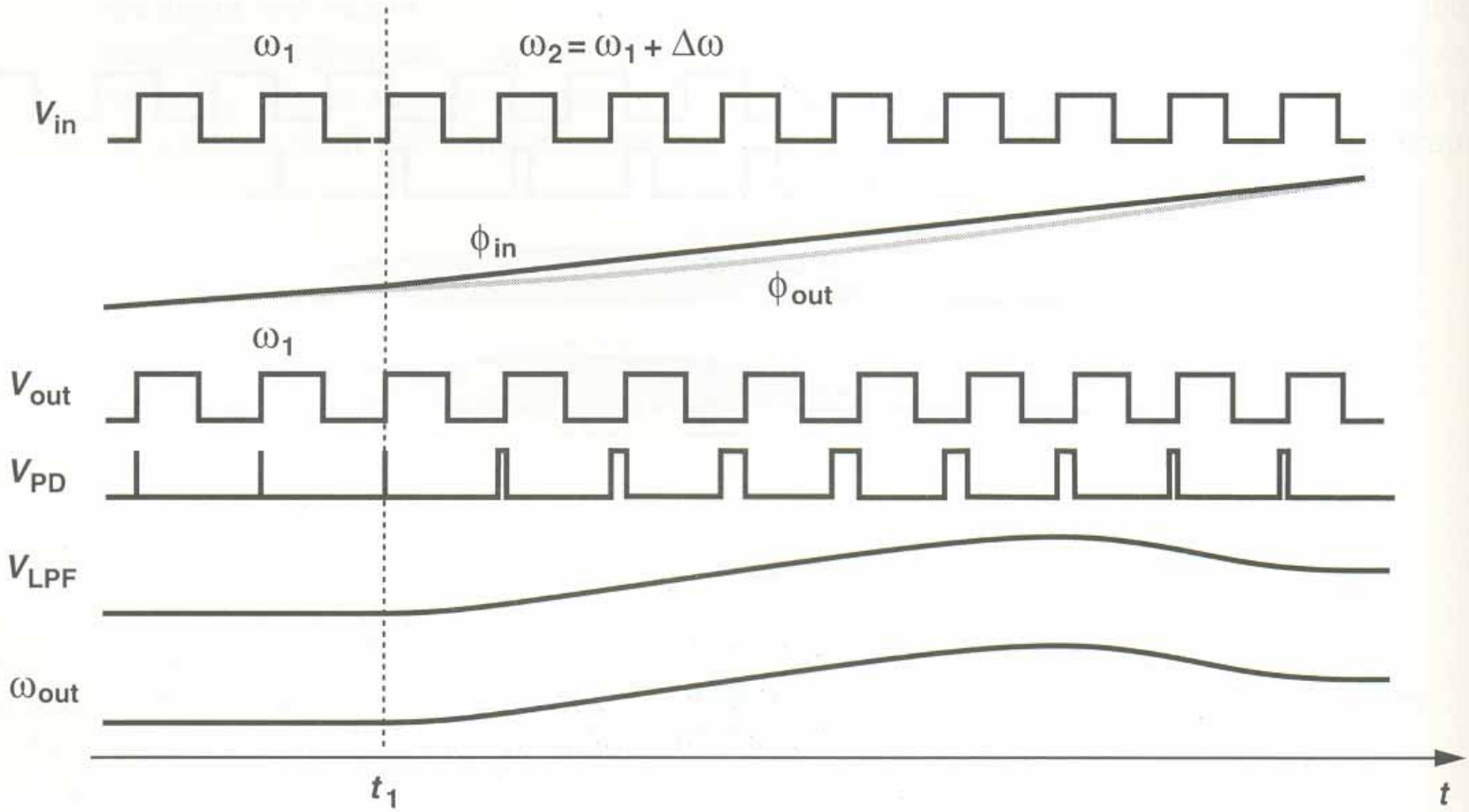


Figure 15.12 Response of a PLL to a small frequency step.

Overcoming the problem of limited acquisition range in Type I PLLs

In order to remedy the acquisition problem, modern PLLs incorporate frequency detection in addition to phase detection. Called "aided acquisition" and illustrated in Fig. 15.21, the idea is to compare ω_{in} and ω_{out} by means of a frequency detector, generate a dc com-

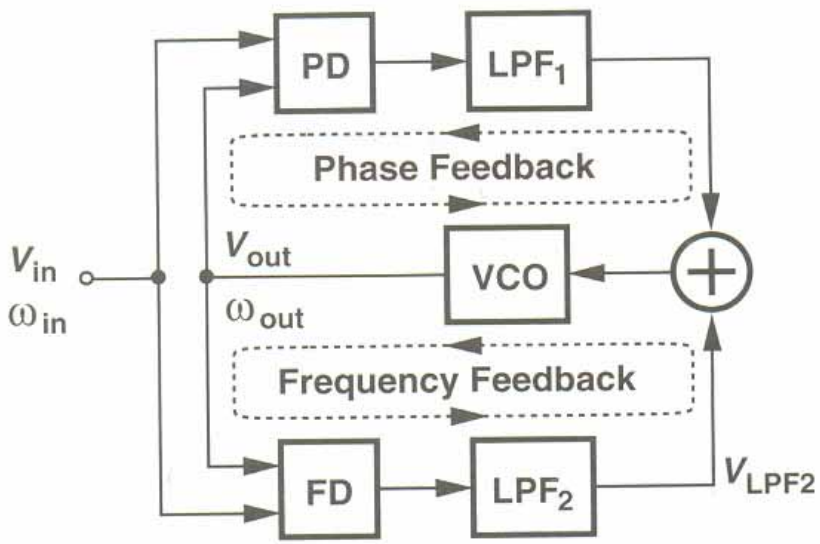


Figure 15.21 Addition of frequency detection to increase the acquisition range.

ponent V_{LPF2} proportional to $\omega_{in} - \omega_{out}$, and apply the result to the VCO in a negative-feedback loop. At the beginning, the FD drives ω_{out} toward ω_{in} while the PD output remains "quiet." When $|\omega_{out} - \omega_{in}|$ is sufficiently small, the phase-locked loop takes over, acquiring lock. Such a scheme increases the acquisition range to the tuning range of the VCO.[7]

Phase/Frequency Detector (PFD)

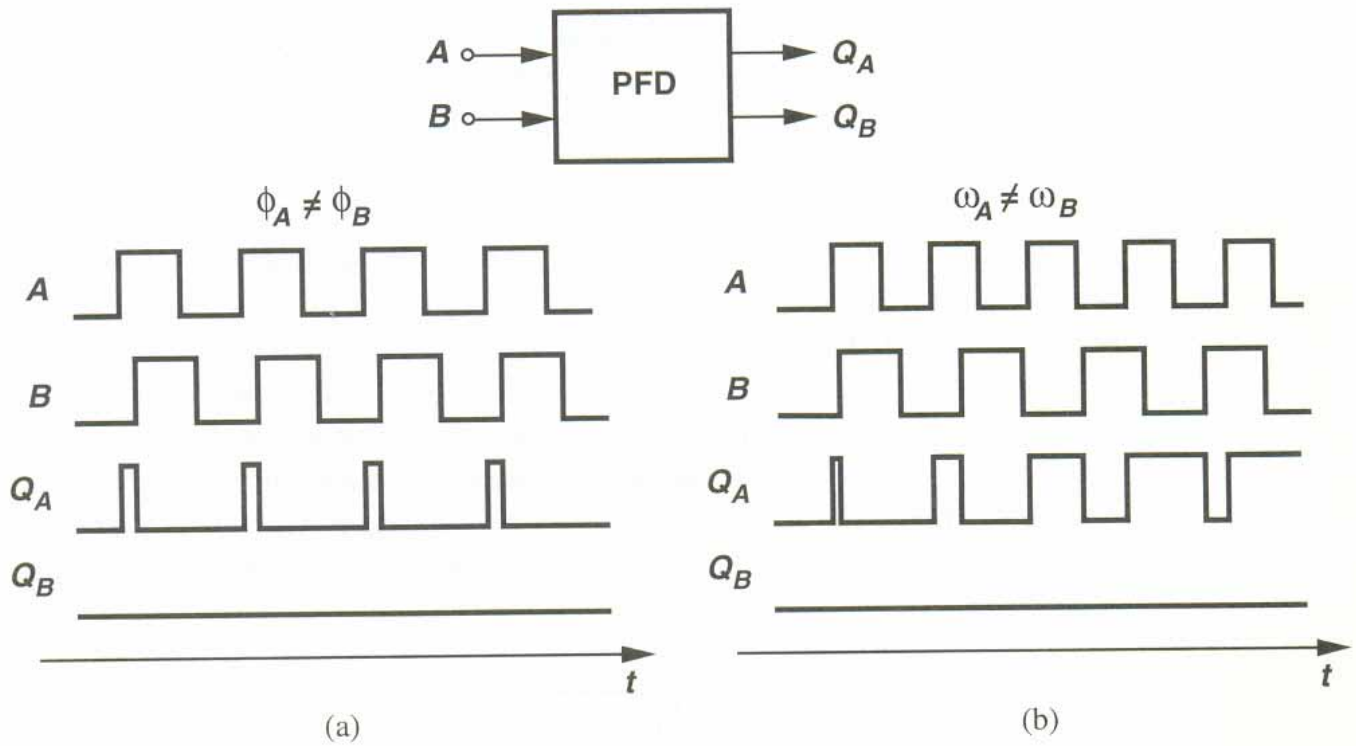


Figure 15.22 Conceptual operation of a PFD.

Phase/Frequency Detector (cont.)

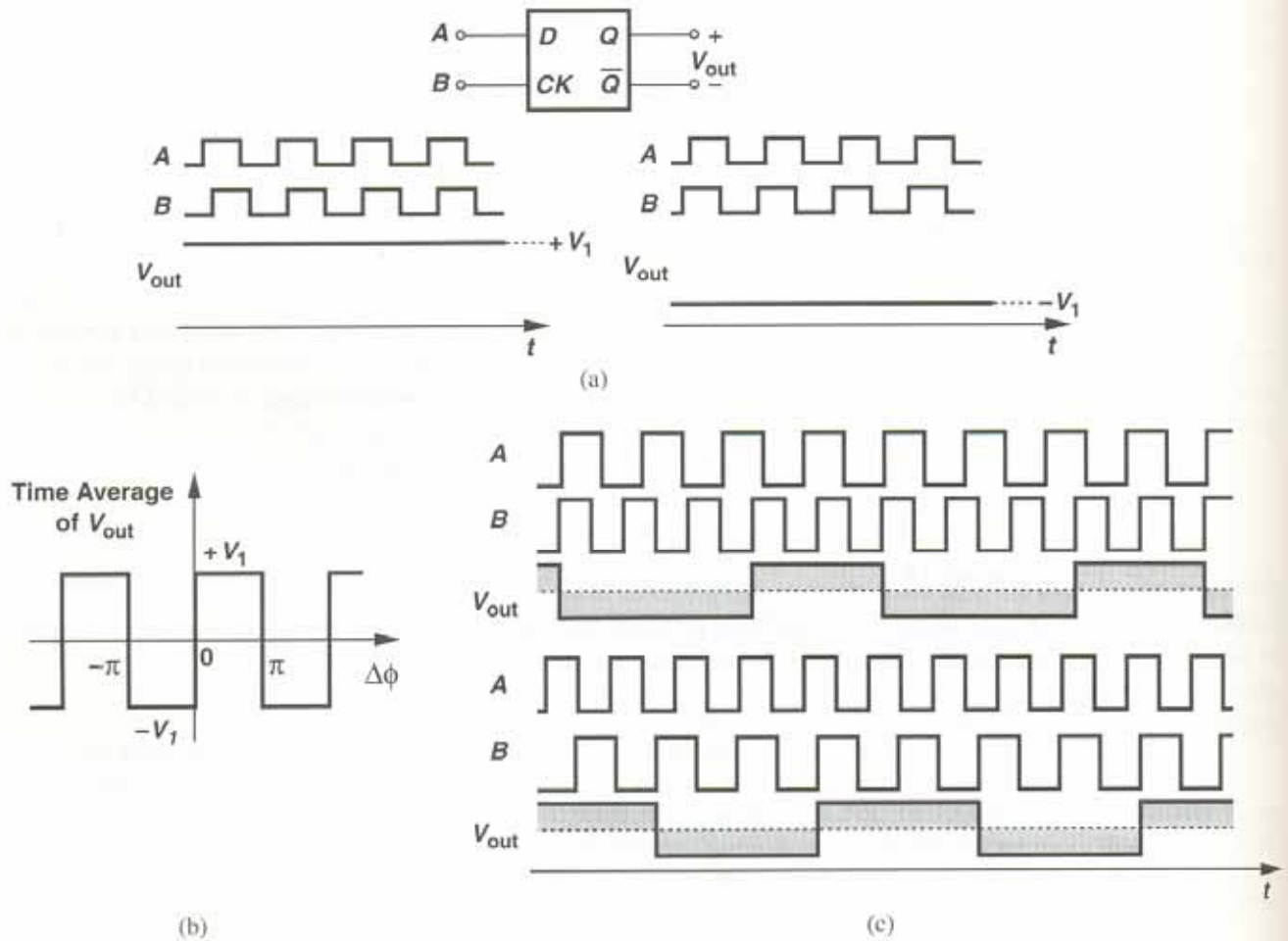
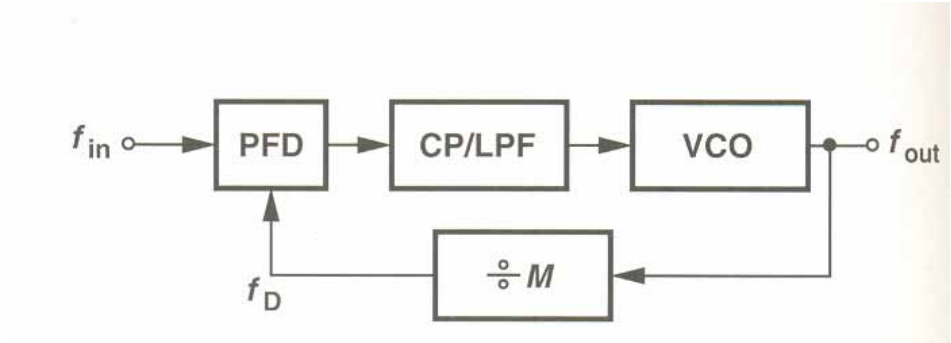
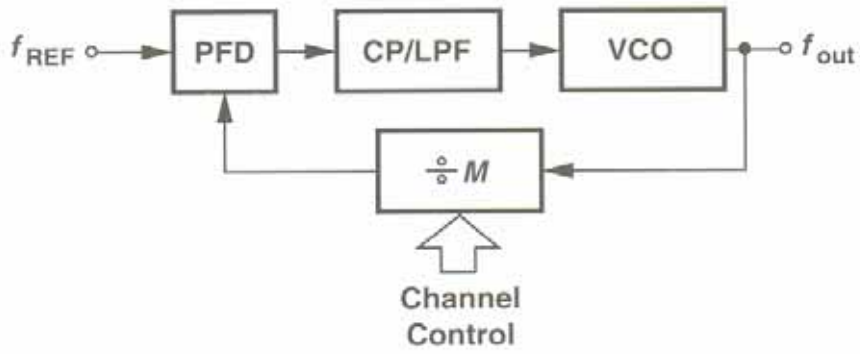


Figure 15.23 (a) D flipflop as a phase detector, (b) input/output characteristic, (c) response of D flipflop to unequal input frequencies.

Applications

Frequency multiplication



Frequency synthesizer